We Claim:

1. A semiconductor memory, comprising:

first lines running along in a first direction;

second lines running along in a second direction and crossing said first lines; and

a configuration of memory cells connected to said first lines and to said second lines, each of said memory cells having a storage capacitor and a vertical selection transistor, each of said memory cells connected at each crossover point between one of said first lines and one of said second lines, each of said second lines connecting together said memory cells whose said storage capacitors are disposed alternately on both sides of a respective second line in a manner laterally offset relative to said respective second line.

2. The semiconductor memory according to claim 1, wherein any two of said memory cells whose said storage capacitors are most closely adjacent to one another are always connected to two mutually adjacent ones of said first lines.

3. The semiconductor memory according to claim 1, wherein any two of said memory cells which are both connected to a respective first line and whose said storage capacitors are

adjacent to one another along said respective first line are always connected to two mutually adjacent ones of said second lines.

4. The semiconductor memory according to claim 1, wherein mutually adjacent ones of said second lines are disposed in a manner offset with respect to one another by twice as large a distance as said first lines that are most closely adjacent to one another.

5. The semiconductor memory according to claim 1, wherein said first lines are bit lines and said second lines are word lines.

6. The semiconductor memory according to claim 5, wherein said storage capacitors of said memory cells are connected to a single respective word line and are disposed alternately on one side of said respective word line and on another side of said respective word line.

7. The semiconductor memory according to claim 1, wherein said first lines are word lines and said second lines are bit lines.

8. The semiconductor memory according to claim 1, wherein said storage capacitors that are most closely adjacent to one

another form a diagonal grid relative to a course of said first lines and relative to a course of said second lines.

9. The semiconductor memory according to claim 1, further comprising a semiconductor substrate and said storage capacitors are trench capacitors buried in said semiconductor substrate.

10. The semiconductor memory according to claim 5, wherein said selection transistors are MOSFETs having gate electrodes connected to said word lines.

11. The semiconductor memory according to claim 1, wherein the semiconductor memory is a dynamic random access memory.